

## CLAIMS

What is claimed is:

1. A method of performing a pipelined arithmetic function comprising  
5 the steps of:

a) receiving two N-bit operands into each of a plurality of adder  
elements in separate pipelines;

b) performing an add operation in each of said plurality of adder  
elements wherein a first N-bit result and a first carry bit is output from each of  
10 said adder elements;

c) receiving said first N-bit result from each of said adder elements  
into a respective N-bit result register and receiving said first carry bit from each of  
said adder elements into a respective carry bit register;

d) outputting from an incrementor in one of said pipelines, a  
15 second N-bit result and a second carry bit from the combination of a first result  
from a first of said N-bit result registers, a first carry bit from a first of said carry bit  
registers, and a first carry bit from a second of said carry bit registers from a  
second of said pipelines; and

e) supplying a final result being a combination of said second N-bit  
20 result from said incrementor, said second carry bit from said incrementor, and  
said first N-bit result from a second N-bit result register in said second pipeline.

2. The method as recited in Claim 1, wherein said N-bit result registers are single width registers.

3. The method as recited in Claim 1, wherein said carry bit registers  
5 are single bit registers.

4. The method as recited in Claim 1, wherein step c) further comprises respectively receiving said first N-bit result into a plurality of single width N-bit registers.

10 5. The method as recited in Claim 1, wherein step c) further comprises respectively receiving said first carry bit into a plurality of single bit registers.

15 6. The method as recited in Claim 1, wherein step d) further comprises respectively receiving said second N-bit result into a plurality of single width N-bit registers.

7. The method as recited in Claim 1, wherein step d) further  
20 comprises receiving said second carry bit into a plurality of single bit registers.

8. A pipelined adder/subtractor comprising:

a) a plurality of adder elements coupled to a plurality of input busses and operable to perform add/subtract operations upon a pair of N-bit operands received from said input busses and storing an N-bit result;

b) a carry bit register coupled to each of said adder elements and  
5 for receiving a carry bit from said adder element;

c) an incrementor coupled to a first of said adder elements, a first of said carry bit registers, and a second of said carry bit registers, said incrementor having an N-bit result output and a carry bit output; and

d) an output bus coupled to said N-bit result output of said  
10 incrementor, said carry bit output of said incrementor, and a second of said incrementor elements.

9. The pipelined adder/subtractor of Claim 8, wherein said plurality of adder elements store said N-bit results in respective single width registers.

10. The pipelined adder/subtractor of Claim 8, wherein said carry bit registers are single bit registers.

11. The pipelined adder/subtractor of Claim 8, further comprising a  
20 plurality of N-bit registers for respectively receiving said first N-bit result from said plurality of adder elements.

12. The pipelined adder/subtractor of Claim 11, wherein said plurality of N-bit registers are single width registers.

13. The pipelined adder/subtractor of Claim 8, further comprising a plurality of N-bit registers for respectively receiving said second N-bit result from said second N-bit output of said incrementor.

14. The pipelined adder/subtractor of Claim 13, wherein said plurality of N-bit registers are single width registers.

15. The pipelined adder/subtractor of Claim 8, further comprising a plurality of said carry bit registers for respectively receiving said carry bits from said adder elements and said incrementor.

16. A multistage adder/subtractor circuit comprising:  
a) a plurality of pipelines connected to a plurality of input busses, each of said pipelines being divided into clock regulated stages and having in its first stage an adder element comprising:

an adder for receiving a pair of N-bit operands and outputting a first N-bit result and a first single bit carry; and  
a single width N-bit register for receiving said first N-bit result from said adder;

and at least one of said pipelines comprising, in a stage  
subsequent to said adder element stage, an incrementor element comprising:

an incrementor for receiving one of said first N-bit results  
and two of said first single bit carries and outputting a second N-bit result and a  
5 second single bit carry; and

a single width N-bit register for receiving said second N-bit  
result;

b) a plurality of single bit registers for receiving said carry bits; and

c) an output bus connected to said pipelines for supplying a final  
10 result being a combination of said first N-bit result, said second N-bit result, and  
said second single bit carry.

17. The pipelined adder/subtractor of Claim 18, further comprising a  
plurality of single width N-bit registers for respectively receiving said first result  
15 from said plurality of adder elements.

18. The pipelined adder/subtractor of Claim 18, further comprising a  
plurality of single width N-bit registers for respectively receiving said second  
result from said incrementor elements.

19. The pipelined adder/subtractor of Claim 18, further comprising a  
plurality of said carry bit registers respectively receive said carry bits from said  
adder elements and said incrementor elements.